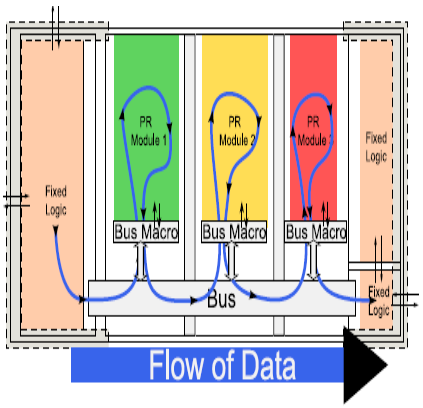
Introduction to Reconfigurable Computing

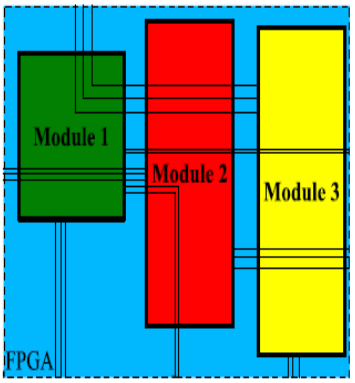
Chapter 6: Online communication

Contents

What is communication?

- Enable the communication at run-time between modules on the chip





1. Direct communication – Similar with the mesh circuit

- Allows modules to communicate using dedicated physical channels
- Configured at compiler time
- Defines the set of physical lines, direction, bandwidth and speed

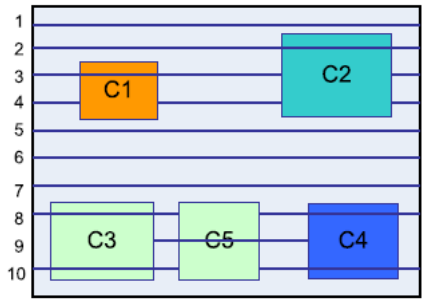


Figure 6.1. Direct communication between placed modules on a reconfigurable device

Line 3: C2 to pins.
Line 4: C1 and C2 for a direct communication.
Lines 8 and 10: C5 to pins. They cross components C3 and C4.
Line 9: connect C3 and C4 and runs through component C5.

Disadvantage

- Dedicated channels must be foreseen to allow signals not used by this component to cross.
- Increases resources, complexity
- Additional restrictions like the availability of signals in a given location.

2. Communication Over Third Party

- A central component exists that behaves as a message reflector.
- Each message is first sent to the central module, which forwards it to the destination

2. Communication Over Third Party(cont)

- Brebner:
  - Uses this approache to allow the communication between a reconfigurable module connected to a processor through a bus and a user program running on the host processor.

2. Communication Over Third Party(cont)

- The module inputs and outputs are controlled by registers that are mapped into the address space of the processor
- Can be used to allow the communication between :
  - a reconfigurable module and a user program
  - between several reconfigurable modules connected together through a bus.

2. Communication Over Third Party(cont)

- The system is controlled by an operating system, whose role is:
  - manage the device resources,
  - control the reconfiguration process
  - allow the communication to happen between the components temporally placed on, or removed from the device.

2. Communication Over Third Party(cont)

- All modules willing to send a message must first copy those messages in their sending register. Thereafter, the operating system copies the message from those registers to the input register of the destination module.

2. Communication Over Third Party(cont)

Walder et al. :

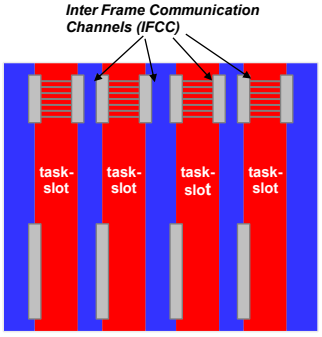
- the central module:
  - not an operating system running on a separate processor.
  - a set of fixed resources on the device.
  - provides dedicated channels to access peripheral devices and also to connect direct neighbour modules.

2. Communication Over Third Party(cont)

- The communication between non-adjacent modules is done through fixed resources implemented on the device

2. Communication via third party

- Encapsulating the BUS-transaction in a wrapper (Brebner, Walder)
  - Divide the device into slots
  - Each task must be placed in a given slot
  - A slot is enveloped in a wrapper which hides the bus-transaction process
- Communication takes place through a fixed module called the OS.
  - Each module can send a message by writing in its send buffer
  - The OS copies messages from the send buffers to the receive buffers of modules
  - The receive modules reads its message from its receive buffer

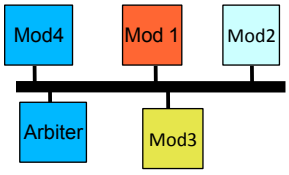


3. Bus-based Communication

- The communication between modules using a common bus
- Only one medium/bus required for all component → Reduces the amount of resources
- Additional delay increased by the bus arbitration that manages the bus access

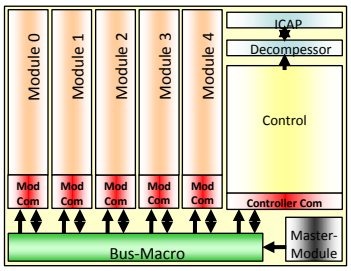
3. BUS - oriented communication

- Many components connected at fixed locations
- One arbiter for BUS-Management
- SoC (System on Chip) Buses can be used to connect different modules
  - ARM AMBA
    - Advance high-performance bus (AHB)
    - Advance peripheral bus (APB)
  - IBM CoreConnect
    - Processor local bus (PLB)
    - On-chip peripheral bus (OPB)
  - Silicore Whisbone



3. BUS - oriented communication

- Using standard bus-arbiter
  - Device is divided into slots
  - Each task must be placed in a slot
  - Each component implements the bus-transaction
  - Each component can be a master
  - An arbiter manages the bus-assignment



Quelle: ITIV, Uni Karlsruhe (TH)

4. Circuit Switching – *Similar with TDM*

The art of dynamically establishing a connection between two processing elements (PE) at run-time

Using a set of physical lines connected by switches.

Switches are at the column and line intersection

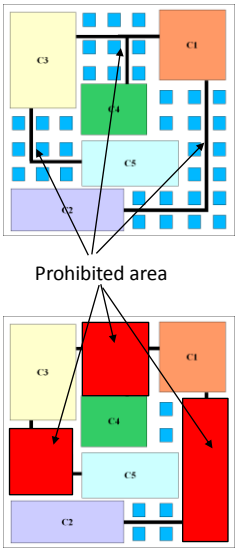
Longer connection using the vertical and horizontal lines at an intersection point.

Two arbitrary PE dynamically connected at run-time by dynamically setting the switches on the path from the first processor to the second one.

Connection is established → data transmitted from the source PE to the destination

4.1 Circuit Switching

- Architecture:
  - Set of Processing elements
  - Communication signals is set between two PEs using a set of switches on a path from the source to the destination
  - Advantage:
    - Direct communication. No need to process packets
  - Drawbacks:
    - Computing a route is expensive. Difficult to be done on-line
    - Routed lines create a large amount of prohibited area
  - Prohibited area can be overcome by using an extra layer exclusive for circuit routing



4.1 1-D Circuit Switching
Reconfigurable multiple bus (RMB)

- A set of switches, locally attached to a component using vertical lines.
- Connection between the switches is a bus
- Bus consists of a set of segmented horizontal lines.

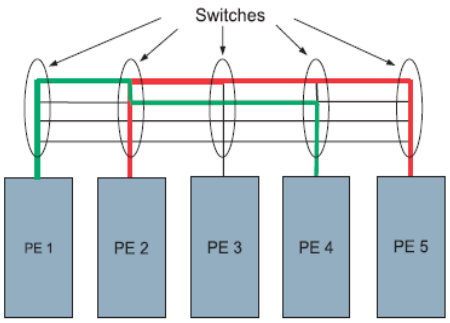
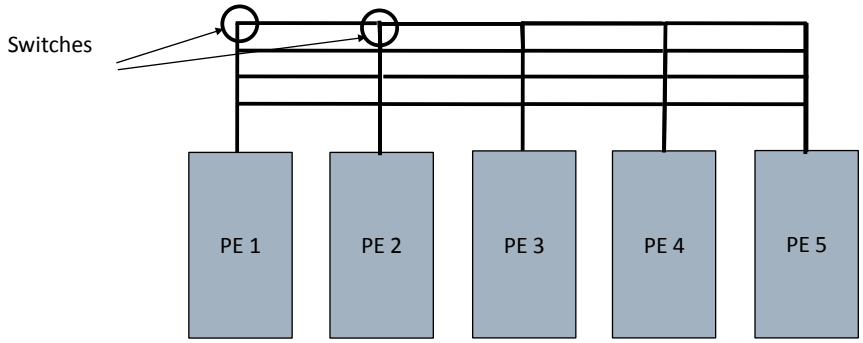


Figure 6.3. The RMBoC architecture

- The switches allow component (say I/O component) to access bus
- Establish communication other components.

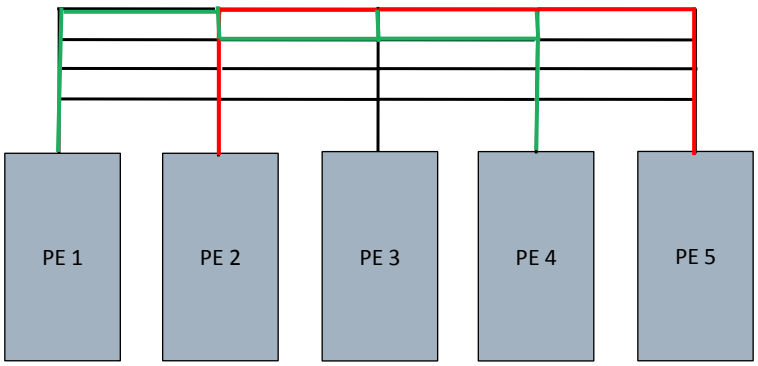
4.2 The reconfigurable multiple bus (RMB) approach

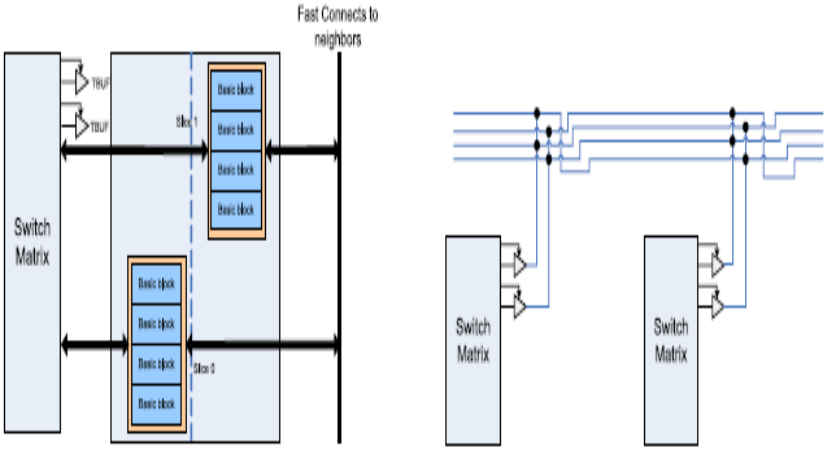
- A set of n processing elements and k segmented buses
- Crosspoints (switches) are used to set the connection between the segments at the run-time



4.2 The reconfigurable multiple bus (RMB) approach

- The sender always initiates and destroy a communication request
- Each communication path is granted until the end of the communication





(a) CLB connexion to the switch matrix (b) Tri-state buffer connection to horizontal lines

Figure 2.30. Virtex routing resource

A sender components *Pk*, position *k* to establish a communication with a receiver component *Pt* , position *t:*

- first send a request to its own switch at location k.
- Switch k forwards the request to switch k + 1
- Switch k + 1 forwards the request to switch k + 2,
- until the request arrives at the switch t

Otherwise, the switch sets the connection and sends an acknowledge.

- The first acknowledge by the last switch t sent back to switch $t - 1$
- Switch $t - 1$ send the acknowledgement to switch $t - 2$
- The process is repeated until the switch at the sender location
- Sender receiving the ACK, the sender can start with the communication

4.1.2 RMBoC on the Xilinx Virtex FPGAs

A uniform interface is for connecting their modules on the Bus.

Modules: can then be placed only on the foreseen slots , or a given amount of consecutive slots.

Bus macros: The segmentation in slots is enforced using dedicated modules, the so-called bus macros, at the boundaries of the slots.

A bus macro is a special hardware module that allows established connections between neighbour component.

Crosspoint: locally manages the connection of the component to the Bus as well as the setting of switches according to the requests and the availability of the channels.

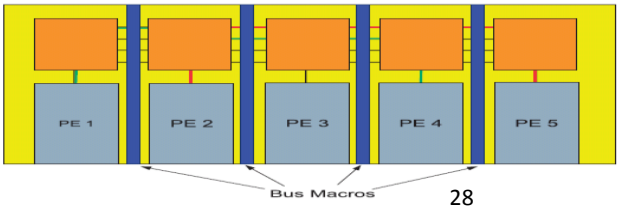


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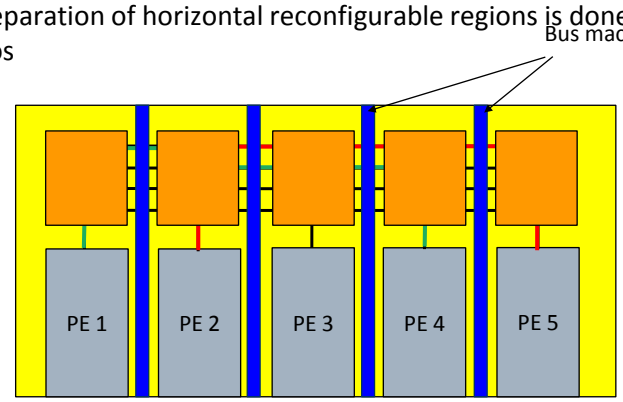
Figure 6.4. RMBoC FPGA implementation

4.2 The reconfigurable multiple bus (RMB) approach

- On a column wise reconfigurable device, the RMB provides a modular communication infrastructure
- All the switches in one column are grouped together
- The separation of horizontal reconfigurable regions is done via bus macros



Crosspoint in RMBoC

Controller:

Manage requests from the left or the right crosspoint and local module.

A communication process starts by a REQUEST command from the sender to its local corresponding crosspoint with the destination address.

The command is successively sent to the next crosspoint in the destination direction until the receiver location or the earliest crosspoint with no free channel.

Upon reaching the destination, a connection will be established and a REPLY is sent back

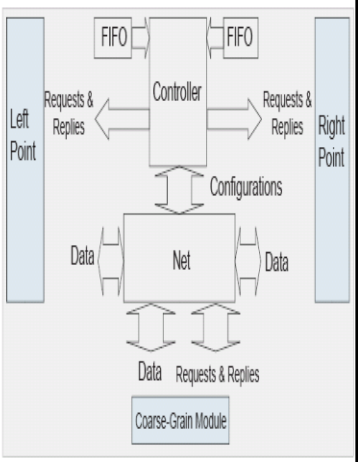


Figure 6.5. Crosspoint architecture

Data network: connect corresponding data channels

FIFOs: buffer for commands

5. Network on Chip- why?

Advantage:

Wiring modules will not be a viable solution in the billion transistor chips

NoC is ultimate solution to avoid problems of the growing size of the chip

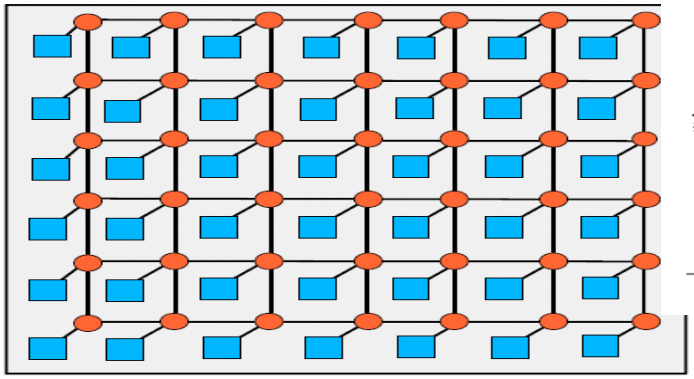
Proposed Network on Chip (NoC) as a good solution to support communication on System on Chip.

NoCs encounter many advantages (performance, structure and modularity) towards global signal wiring.

5. Network on Chip – *Similar with network*

NoC architecture is routers

Network topology is arrangement of routers attaching to PE and processor



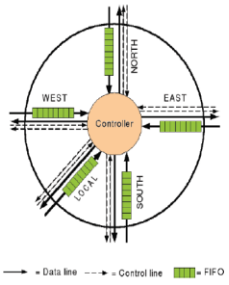


Figure 6.7. Router Architecture

= PE = Network logic (Router) = Network

Figure 6.6. A Network on Chip on a 2-D Mesh

A chip employing an NoC consists of a set of network clients such as DSP, memory, peripheral controller, custom logic

Communicate on a packet base instead of using direct connection.

Components just send packets

Do not care on how the packets are routed

5.1 The Processing Element (PE)

A processing element can be:

- a processor core
- a memory block
- an embedded programmable logic
- any custom hardware block.

Processing elements connected to router through an interface

Each processing element has a unique address

5.1.1 Wrapper

A wrapper is to decouple the network activities from the computation within a processing element.

The wrapper controls all the transaction on the network

Provides a simple interface to access the network.

Incoming packets has address along with the payload.
This address is removed in the wrapper, and only the payload is passed to the PE.

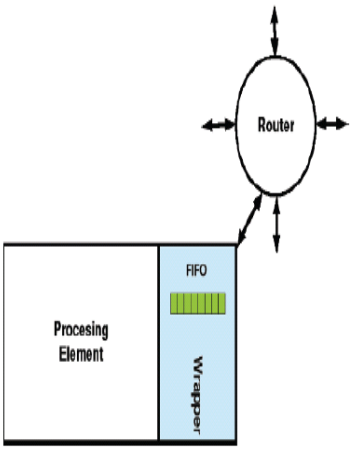


Figure 6.11. A general wrapper architecture

5.2 The Router

The basic blocks of an NoC are routers that consist of :

- Buffers: a given set of component to temporarily store packets.

- Controller: determines how to forward the packets

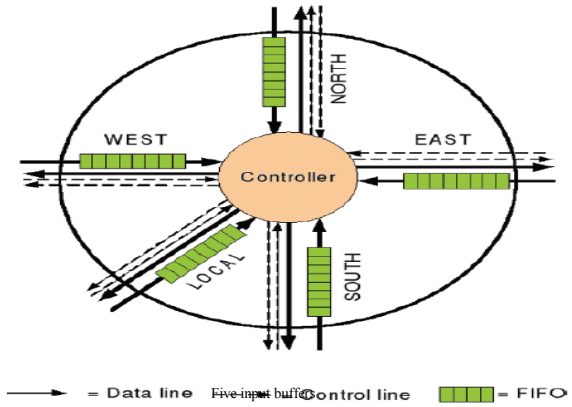
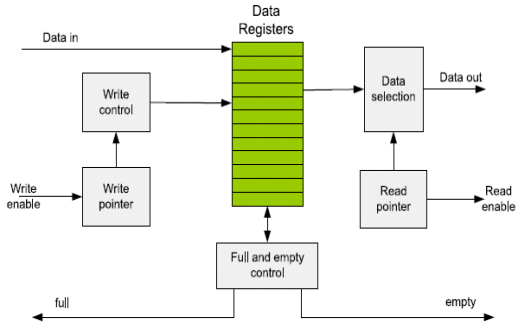


Figure 6.7. Router Architecture

Five input buffers implemented as FIFOs
Controller manages the dataflow
Five Output Arbiters manage the message to output channels

The FIFO in Router



FIFO is a data storage to model a queue

A set of registers in serial way for storing the data.

Data to be shifted from one register to the next one.

Data are written on one side and read from the other side

Router Control

Each router has position (x,y)-coordinate of the processing element on which the router is attached.

Messages : address of destination router, control bits and the payload (data).

The first part is the packet address: determine the direction where to send the packet.

Decodes the address into (x,y) coordinate of destination router or PE.

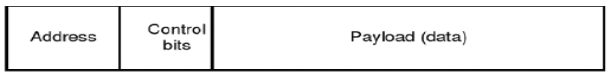


Figure 6.9. General format of a packet

Output Arbiter in Router

A simple arbiter may consists of a multiplexer and a Finite State Machine

Data written with order EAST, WEST, SOUTH, and NORTH

The incoming packets from the EAST will be written before the one coming from the WEST, then from SOUTH, then from NORTH.

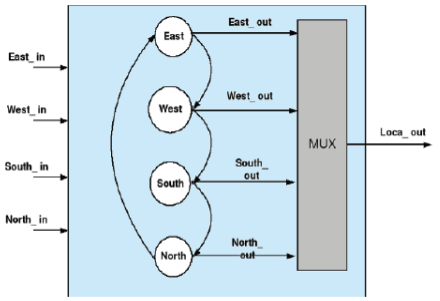


Figure 6.10. Arbiter to control the write access at output data lines

Routing Technique – Circuit Switching

Approach allows a communication path to be created from the source to the destination before transmitting any data.

The procedure starts :

- a routing probe traversing the network and reserving links to transmit the data.
- This routing probe contains the source and destination addresses.
- Once the routing probe reaches the destination address, an acknowledgment is sent back to the source address
- Data are transferred at the full bandwidth of the hardware.

The disadvantage is the time required to establish a dedicated link from source to destination. It can be advantageous when the time to set up the path is minimal, compared with the transfer time of the messages

Routing Technique – Store-and-Forward

- At each node, the packets are stored in memory

- The routing information examined to determine which output channel to direct the packet.

- The technique is referred store-and-forward (SAF).

Latency for a packet is the number of routers * time to transfer the packet between the routers.

Routing Tech – Virtual Cut-Through

Address deficiency in SAF-based: buffering of messages at each node

Packet should not be stored in the current node's memory if an output buffer is available.

The packet simply cuts through the router of the node to an available output channel.

Routing Tech – Wormhole Routing

Address the deficiency in VCT, that is, if an output channel is not available, the packet must be stored in the current node's memory.

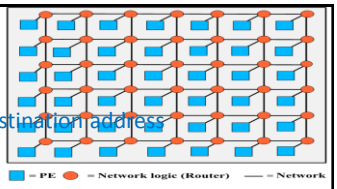
Divides a message into smaller flow-control digits than packets, which are called flits. Each message contains one header flit , data flits.

The header flit always goes first to allocate a path for the data flits. Smaller memory requirements exist (buffers flits instead of packets).

If an output channel is available, the header flit is routed and the remaining data flits follow in a pipeline style fashion. During any instance of a message traversing a network, the flits of a message will be located in multiple routers

Looks like a worm traversing the network. Benefits from very low latency and buffer space, blocking and deadlock problems can occur.

5.5 Deterministic XY-Routing



The XY-routing algorithm routes the packets based on the destination address

In a 2-D mesh network:

- XY-routing first routes packets along the X-axis to reaches the destination's column
- the packet is then routed along the Y-axis until the destination's line.

The router compares its own address (Xrouter, Yrouter) to the destination address of a packet. Packets are forwarded based on destination address (Xdest, Ydest) as follows.

- If Xrouter < Xdest, the packet -→ forwarded in the east direction
  If Xrouter > Xdest, the packet -→ forwarded in the west direction
  If Xrouter = Xdest and Yrouter > Ydest -→ sent to the south of the current router
  If Xrouter = Xdest and Yrouter < Ydest, →sent to the north of the current router
  If Xrouter = Xdest and Yrouter = Ydest, the packet is sent to the local PE

5.6 Adaptive Routing

Adaptive algorithms: - performance in the presence of localized traffic

- provide fault-tolerance in the network.

1. Packets are not always routed along the shortest path.

2. If deadlock and livelock problems , The longest routing path may be prefered

These delivery times are updated every time a router forwards a packet. On the basis of this information, a router can choose an alternative route when the queues are congested in the intermediate routers,

Resulting in faster delivery compared to the XY-routing algorithm.

6. The Dynamic Network on Chip (DyNoC)

In a DyNoC, a routers is :

- a programmable element basically configured as router

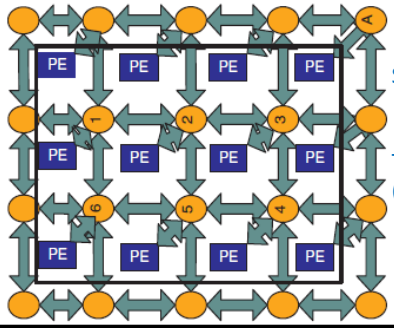
- can be configured at run-time to implement any function that can fit on it

Why DyNoC ?

First, the components fits on one PE, place the component on one PE and attach it to the corresponding router to communicate with other components.

Component need more PE: the component will be splitted in pieces, each of on a PE.

The communication between the pieces on different PE will use the router network →wasted



Solution: connect all the PE using direct wiring.

The routers inside the area of the components (1,2,3,4,5,6) become redundant.

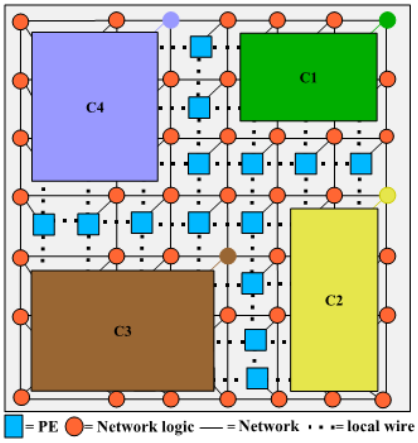
Why DyNoC ?

In a DyNoC, a routers is a PE configured at run-time

Redundant routers → additional resources for the module.

Direct communication lines exist between neighbour PEs

Whenever a component is placed in a given region, only one router is necessary for this element to access the network.



Activated and deactivate routers

Routers notify their neighbours about their activity using an additional activation line that is set to one if the router is active

As those routers cannot be used, they are deactivate.
The component therefore sets the activation signal to the neighbour routers to notify them not to send packets in its direction.

Definition 6.1: A component (pin) is reachable if each message sent to this component (pin) can reach the component (pin).

Definition 6.2: The device is strongly connected if for each pair of components A and B, a path of active routers that connects the two components

→each component must always be surrounded by a ring of active routers

Theorem 6.3: If each component is synthesized and is internally surrounded only by processing elements, then all placements on the reconfigurable device are strongly connected.

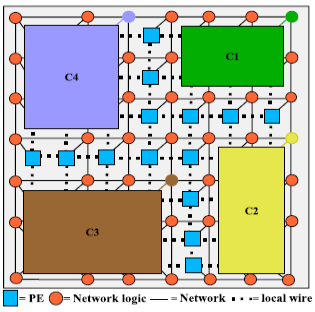
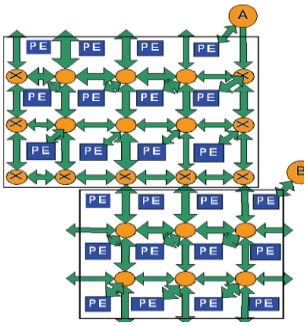


Figure 6.15. A strongly connected configuration on a DyNoC

No route is available between those two component, because the only routers available are consumed by the first component.



Therefore, no matter where a component is placed on the device, it will always be surrounded by a ring of routers.

After the placement of a new component on the device at run-time, its coordinate is set to that of its corresponding router.

6.3 Routing Algorithm in DyNoC

Adaptive routing algorithms. The strategy is based on the XY-routing.

The adapted XY-routing in three different modes:

The N-XY (Normal XY) mode when all the neighbours of a routers are active

The SH-XY mode: The router enter this mode when its left neighbour or its right neighbour is deactivated.

The SA-XY mode: The router enter this mode when its upper neighbour or its lower neighbour is deactivated.

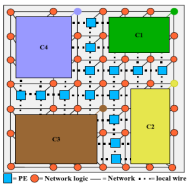


Figure 6.15. A strongly connected configuration on a DyNoC

The SH-XY mode: Surrounding Obstacles in the X-direction

According to the XY-routing, packet is sent upward if the Y-coordinate of destination of the packet is greater than that of the router.

Otherwise, the second path is chosen and the packet is sent downward.

The SA-XY mode :Surrounding Obstacles in the Y-direction

Packet will be sent left or right

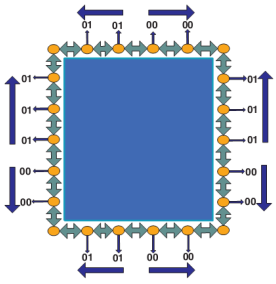


Figure 6.19. Router guiding in a DyNoC

6.3.3 Router Guiding

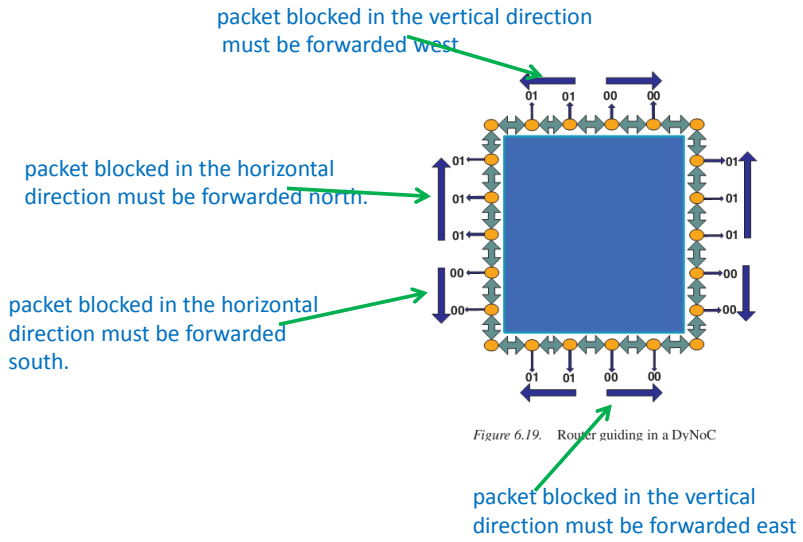


Figure 6.19. Router guiding in a DyNoC

The end of the presentation

THANK YOU