



**Vietnam National University – Ho Chi Minh City
Ho Chi Minh City University of Technology**

**The Second
Symposium on**

**Computer Science
and Engineering**

Proceedings

**SCSE
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Ho Chi Minh City University of Technology



SYMPOSIUM ON COMPUTER SCIENCE AND ENGINEERING

SCSE 2021

Ho Chi Minh City, Vietnam

October 22-23, 2021

MESSAGE FROM THE GENERAL CHAIRS

SCSE 2021 is a forum for the exchange of ideas, techniques, and state-of-the-art applications in the fields of computer science & engineering among scientists, engineers, and practitioners. For SCSE 2021, we will provide a friendly environment where researchers can discuss current and future trends in research areas such as Applied Artificial Intelligence, Image Processing and Visualization, Embedded Systems and VLSI Design, High Performance Computing, Internet of Things, Network and Service Management and other interesting topics.

SCSE 2021, hosted by Faculty of Computer Science & Engineering, is the second symposium in conjunction with the 17th Science and Technology Conference of Ho Chi Minh City University of Technology (HCMUT), Vietnam from October 22-23, 2021. In SCSE 2021, we selected 12 papers to appear in a special issue of REV Journal on Electronics and Communications (ISSN: 1859-378X), published by The Radio and Electronics Association of Vietnam. This year, we also invited 2 keynote speakers from Australia and Japan, and organized an industrial workshop on “Digital Transformation-- Practical Views”.

We would like to thank the SCSE 2021 organizing committee members, the technical program committee members for their tremendous contributions. Finally, we would like to acknowledge the keynote speakers, the industrial workshop speakers, the authors, and all attendees for their great contribution and participation.

Pham Tran Vu

Tran Ngoc Thinh

Tran Manh Ha

Pham Quoc Cuong

HCMC, October – 2021

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TABLE OF CONTENTS

MESSAGE FROM THE GENERAL CHAIRS	I
COMMITTEES	II
INDUSTRY WORKSHOP	1
KEYNOTES.....	2
AN EFFICIENT APPROACH TO MEASURE THE DIFFICULTY DEGREE OF PRACTICAL PROGRAMMING EXERCISES BASED ON STUDENT PERFORMANCES	4
HUY TRAN, TIEN VU VAN, HOANG NGUYEN VIET, DUY TRAN NGOC BAO, THINH TIEN NGUYEN, AND THANH VAN LE.....	4
INFECTIOUS DISEASE SCREENING SYSTEM USING MEDICAL RADAR AND DATA QUALITY ASSESSMENT BY EFFICIENT NEURAL NETWORK HARDWARE	5
DUC-THO MAI, KOKI KUMAGAI, GUANGHAO SUN AND KOICHIRO ISHIBASHI	5
GENERATING WEBSITE CODES FROM IMAGES.....	6
LAI NGUYEN HA MY, HUYNH NGOC THIEN, AND NGUYEN DUC DUNG	6
AN EFFICIENT HARDWARE IMPLEMENTATION OF CONVOLUTIONAL NEURAL NETWORK IN DETECT BREAST CANCER HISTOPATHOLOGY IMAGE.....	7
VO TAN PHAT, AND HOANG TRANG	7
A MULTITASK DATA-DRIVEN MODEL FOR BATTERY REMAINING USEFUL LIFE PREDICTION.....	8
THIEN PHAM, LOI TRUONG, MAO NGUYEN, ANH BUI, DANG NGUYEN, DAT NGUYEN, AKHIL GARG, LIANG GAO, AND THO QUAN	8
NEIGHBORHOOD SEARCH FOR SOLVING PERSONAL SCHEDULING PROBLEM IN AVAILABLE TIME WINDOWS WITH SPLIT-MIN AND DEADLINE CONSTRAINTS.....	9
TRANG HONG SON, TRAN VAN LANG, AND NGUYEN HUYNH-TUONG	9
AN FPGA-BASED CONVOLUTION IP CORE FOR DEEP NEURAL NETWORKS ACCELERATION ...	10
XUAN-QUANG NGUYEN, AND CUONG PHAM-QUOC	10

PGN-LM MODEL AND FORCING-SEQ2SEQ MODEL: MULTIPLE AUTOMATIC MODELS OF TITLE GENERATION FOR NATURAL TEXT USING DEEP LEARNING	11
NHAN TO, THUAN NGUYEN THI HIEP, AND THO QUAN THANH.....	11
ENHANCING SECURITY AND ROBUSTNESS FOR SDN-ENABLED CLOUD NETWORKS	12
LONG TAN LE, AND TRAN NGOC THINH.....	12
UNBIASED PAIRWISE APPROACH TOWARD LEARNING-TO-RANK: AN EMPIRICAL STUDY	13
SON THANH LE, HA MANH TRAN, QUANG DUY NGUYEN, AND SINH VAN NGUYEN	13
REAL-TIME FACE DETECTION AND HUMAN TRACKING SYSTEM ON FPGA CYCLONE-V	14
HUU LUONG NGUYEN, MINH SON NGUYEN, AND TRI NHUT DO	14
TWO-PHASE DEFECT DETECTION USING CLUSTERING AND CLASSIFICATION METHODS	15
HA MANH TRAN, TUAN ANH NGUYEN, SON THANH LE, GIANG VU TRUONG HUYNH, AND TUAN BAO LAM.....	15

INDUSTRY WORKSHOP

DIGITAL TRANSFORMATION – PRACTICAL VIEWS

In Conjunction with
Symposium on Computer Science & Engineering 2021 (SCSE 2021)



Digital Transformation: Trends, Challenges/Opportunities and Practices

Mr. Phan Thanh Son

Director, Strategic Business, FPT Corporation

Chief Business Development Officer, FPT Information Systems



Digital Transformation in Business Administration – Practical Applications

Dr. Quach Ngoc Long

Founder and CEO of WORKIT

Founder and CEO of EPACIFIC



Towards a Modern Supply Chain Management Platform: Seamless interactivity across the entire supply chain with standardized master data

Mr. Lai Duc Nhuan

Chairman, CEO of ATALINK

Chairman of LARION Computing

Co-founder of MEPERIA



Managing Enterprise's Content in Digital Transformation

Mr. Ho Thai Truong Giang

Co-founder of EyeQ Tech

Co-founder of INTELIN TECHNOLOGY CORP

Used to be Manager of IT and Operations Departments of ACB

KEYNOTES

MCU PROCESS VITAL SIGN ACQUISITION USING CONTACTLESS DOPPLER RADAR

Prof. Koichiro Ishibashi

The University of Electro-Communications, Tokyo, Japan

Abstract

Recently a lot of researchers have investigated Vital Sign Acquisition by Medical Doppler Radar. The vital sign can be acquired contactless manner so that we can easily acquire the vital signs rather than contactless system such as ECC or PPG. This paper demonstrates the signal processing of the vital sign signals on time domain and peak detection. The process is so light that low performance MCU can process them to acquire the vital signs at fast time.

Biography of Prof. Koichiro Ishibashi



Dr. Koichiro Ishibashi has been a professor of The University of Electro-Communications (UEC), Tokyo, Japan since 2011. He has been the Director of UEC ASEAN Research and Education Center (UAREC) since 2017. He has been serving a guest professor at Ho Chi Minh City University of Technology and Ho Chi Minh City University of Science since 2012.

After receiving PH. D degree from Tokyo Institute of Technology in 1985, he worked at Central Research Laboratory, Hitachi Ltd., at Semiconductor Technology Academic Research Center (STARC) and at Renesas Electronics, where he had investigated low power technologies for high density SRAMs and MCUs. Since 2005, he has been a Fellow of IEEE for the technical contributions to developments of low-power SRAMs and MCUs.

He has presented more than 200 academic papers at international conferences and journals including more than 20 invited presentations. He was awarded R&D 100 for the development of SH4 Series Microprocessor in 1999.

His current interests are IoT technologies including Ultra low power LSI design technology, Technologies for energy harvesting sensor networks and applications, and Biomedical electronics using contactless sensors and data processing by AI.

KEYNOTES

AI-EMPOWERED EDGE COMPUTING WITH EFFICIENT AND SECURE DISTRIBUTED LEARNING

Dr. Diep Nguyen

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Abstract

By “moving” computing resources closer to users and infrastructure, edge computing has become an enabler of new emerging services and smart infrastructures like intelligent transportations, industry automation, real-time gaming, virtual/augmented reality. This talk explores how recent advances in distributed learning (DL) can empower edge computing to turn existing infrastructure into smart one with augmented intelligence. Specifically, we first discuss hurdles like low-latency requirement, straggling effect, and users’ security-related risks of DL in wireless edge networks. We then present potential solutions by leveraging coded computing, network economics to address the straggling problem, protect users' privacy, and incentivize users to efficiently contribute to the learning process. We will also present an in-network computation framework to enable large-scale distributed learning systems in wireless edge networks.

Biography of Dr. DIEP NGUYEN



Diep N. Nguyen (Senior Member, IEEE) received the M.E. degree in electrical and computer engineering from the University of California at San Diego (UCSD) and the Ph.D. degree in electrical and computer engineering from The University of Arizona (UA). He is currently a Faculty Member of the Faculty of Engineering and Information Technology, University of Technology Sydney (UTS).

Before joining the UTS, he was a DECRA Research Fellow at Macquarie University, and a member of Technical Staff at Broadcom, CA, USA, and ARCON Corporation, Boston, consulting the Federal Administration of Aviation on turning detection of UAVs and aircraft, U.S. Air Force Research Lab on antijamming.

His current research interests include computer networking, wireless communications, and machine learning applications, with an emphasis on systems performance and security/privacy. He has received several awards from LG Electronics, UCSD, UA, U.S. National Science Foundation, and Australian Research Council. He is an Editor, Associate Editor of the IEEE TRANSACTIONS ON MOBILE COMPUTING, IEEE ACCESS, IEEE SENSORS JOURNAL, and IEEE OPEN JOURNAL OF THE COMMUNICATIONS SOCIETY (OJ-COMS).

AN EFFICIENT APPROACH TO MEASURE THE DIFFICULTY DEGREE OF PRACTICAL PROGRAMMING EXERCISES BASED ON STUDENT PERFORMANCES

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ABSTRACT

This study examines the generality of easy to hard practice questions in programming subjects. One of the most important contributions is to propose four new formulas for determining the difficulty degree of questions. These formulas aim to describe different aspects of difficulty degree from the learner's perspective instead of the instructor's subjective opinions. Then, we used clustering technique to group the questions into three easy, medium and difficult degrees. The results will be the baseline to consider the generality of the exercise sets according to each topic. The proposed solution is then tested on the data set that includes the results of the two subjects: Programming Fundamentals, Data Structures and Algorithms from Ho Chi Minh City University of Technology. The most important result is to suggest the instructors complete various degrees according to each topic for better evaluating student's performance.

Keywords: *e-learning, difficulty degree, automatic question classification, student's perception, effective coverage exercise.*

INFECTIOUS DISEASE SCREENING SYSTEM USING MEDICAL RADAR AND DATA QUALITY ASSESSMENT BY EFFICIENT NEURAL NETWORK HARDWARE

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ABSTRACT

In recent years, various state-of-the-art machine learning algorithms enable improving medical diagnoses and developing efficient tools to process complex biomedical signals. Neural network models demonstrate tremendous efficiency in numerous applications requiring biomedical signal processing due to their pattern-matching capabilities and human brain-like features. Vital signs mixed with noise acquired via the non-contact medical radar method are enormous challenges for researchers who want to analyze and process these signals. This paper presents a hardware architecture of $3 \times 6 \times 5 \times 4$ Neural Networks to take advantage of the hardware resource, enable computation acceleration, and ensure the reliability of classified signals for infectious disease screening systems. The proposed optimized architecture uses a 16-bit floating-point data representation, is synthesized on Xilinx Artix-7 XC7A200T board at a maximum operating frequency of 119.02 MHz, and low hardware resource utilization. The experimental results show that the design can reach about 93% classification accuracy in test results.

Keywords: *Infectious Disease Screening, Neural Networks, Hardware Implementation, Vital Signs, Non-contact Medical Radar.*

GENERATING WEBSITE CODES FROM IMAGES

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ABSTRACT

Brainstorm website layout ideas usually start with everyone giving out their mockups, and all the team members will discuss to finalize the layout of the user interface. Once a vision of that mockup is accepted, it is given to the designer to sketch it digitally on computer software (i.e., Photoshop, Figma, Sketch). When the designer completes, the developer based on the final design to code the UI/UX of the website. As we can see, the process requires three stages, which can be time-consuming. Therefore, if anyone has an idea for the professional website layout, they can visualize it by drawing on sketches. However, it can be impossible for them to make a usable website without designers and website developers. Due to that reason, our primary goal in this paper is to help individuals transform their hand-drawn sketch images into a website that can be deployed. To achieve that goal, we present two approaches: classical computer vision techniques and the other using a deep learning model to detect the sketch and execute the conversion. Furthermore, our evaluation shows that deep learning is the most promising direction. Still, classical techniques also improve the model's input data by applying it in the pre-processing image.

Keywords: *Computer vision, Hand-drawn sketch, UI/UX, Deep learning.*

AN EFFICIENT HARDWARE IMPLEMENTATION OF CONVOLUTIONAL NEURAL NETWORK IN DETECT BREAST CANCER HISTOPATHOLOGY IMAGE

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ABSTRACT

This paper presents our work on evaluating the effectiveness of a novel deep convolutional neural network architecture (CNN) for classifying breast histology images for cancer risk factors as negative or positive. Also, the hardware structure of the proposed model was successfully synthesized and verified. The results indicate that a CNN trained on a small dataset achieved an overall AUC (Area under the receiver operating characteristic curve - ROC Curve) value of 0.922 on a set of 55505 test images. In addition, the time it takes to classify each image is within 3.8 milliseconds instead of a task that even trained pathologists take hours to complete.

Keywords: *Convolutional Neural Network, FPGA, Breast Cancer, Hardware Implementation.*

A MULTITASK DATA-DRIVEN MODEL FOR BATTERY REMAINING USEFUL LIFE PREDICTION

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ABSTRACT

Lithium-ion batteries (LIBs) have recently been used widely in moving devices. Understand status of the batteries can help to predict the failure and improve the effectiveness of using them. There are some lithium-ion information that define the battery health over time. These are state-of-charge (SOC), state-of-health (SOH), and remaining-useful-life (RUL). Normally, a LIB is working under charging and discharging cycles continuously. In this paper, we will focus on the data dependency of different time-slots in a cycle and in a sequence of cycles to retrieve RUL. We leverage multi-channel inputs such as temperature, voltage, current and the nature of peaks cross the cycles to improve our prediction. Comparing to existing methods, the experiments show that we can improve from 0.040 to 0.033 (reduce 17.5%) in RMSE loss, which is significant.

Keywords: *Lithium-ion battery, time-series, Conv2DLSTM, RUL.*

NEIGHBORHOOD SEARCH FOR SOLVING PERSONAL SCHEDULING PROBLEM IN AVAILABLE TIME WINDOWS WITH SPLIT-MIN AND DEADLINE CONSTRAINTS

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ABSTRACT

The scheduling of individual jobs with certain constraints so that efficiency is a matter of concern. Jobs have deadlines to complete, can be broken down but not too small, and will be scheduled into some available time windows. The goal of the problem is to find a solution so that all jobs are completed as soon as possible. This problem is proved to be a strongly NP-hard problem. The implementation of the proposed MILP model using a CPLEX solver was also conducted to find optimal solution for the small-size dataset. For large-size dataset, heuristic algorithms are recommended such as First Come First Served (FCFS), Earliest Deadline (EDL), and neighborhood search including Stochastic Hill Climbing (SHC), Random Restart Hill Climbing (RRHC), Simulated Annealing (SA) to find a good solution in an acceptable time. Experimental results will present in detail the performance among the groups of exact, heuristic, and neighborhood search methods.

Keywords: *splitting-job, available time-window, deadline constraint, FCFS rule, EDL rule, neighborhood search, hill climbing algorithm, simulated annealing algorithm.*

AN FPGA-BASED CONVOLUTION IP CORE FOR DEEP NEURAL NETWORKS ACCELERATION

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ABSTRACT

The development of machine learning has made a revolution in various applications such as object detection, image/video recognition, and semantic segmentation. Neural networks, a class of machine learning, play a crucial role in this process because of their remarkable improvement over traditional algorithms. However, neural networks are now going deeper and cost a significant amount of computation operations. Therefore, they usually work ineffectively in edge devices that have limited resources and low performance. In this paper, we research a solution to accelerate the neural network inference phase using FPGA-based platforms. We analyze neural network models, their mathematical operations, and the inference phase in various platforms. We also profile the characteristics that affect the performance of neural network inference. Based on the analysis, we propose an architecture to accelerate the convolution operation used in most neural networks and takes up most of the computations in networks in terms of parallelism, data reuse, and memory management. We conduct different experiments to validate the FPGA-based convolution core architecture as well as to compare performance. Experimental results show that the core is platform-independent. The core outperforms a quad-core ARM processor functioning at 1.2GHz and a 6-core Intel CPU with speed-ups of up to 15.69× and 2.78×, respectively.

Keywords: *Convolution neural network; Reconfigurable hardware; FPGA design.*

PGN-LM MODEL AND FORCING-SEQ2SEQ MODEL: MULTIPLE AUTOMATIC MODELS OF TITLE GENERATION FOR NATURAL TEXT USING DEEP LEARNING

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ABSTRACT

In the current era, the amount of information from the Internet in general and the electronic press in particular has increased rapidly and has extremely useful information value in all aspects of life, many popular users have posted several high-quality writings as casual blogs, notes or reviews. Some of them are even selected by editors to be published in professional venues. However, the original posts often come without titles, which are needed to be manually added by the editing teams. This task would be done automatically, with the recent advancement of AI techniques, especially deep learning. Even though auto-title can be considered as a specific case of text summarization, this job poses some major different requirements. Basically, a title is generally short but it needs to capture major content while still maintaining the writing style of the original document. To fulfill those constraints, we introduce PGN- LM Model, an architecture evolved from the Pointer Generator Network, with the ability to solve Out-of-Vocabulary problems that traditional Seq2Seq models cannot handle, and at the same time combined with language modeling techniques. In addition, we also introduce a model called Forcing-Seq2Seq Model, an enhanced Seq2Seq architecture, in which the classical TF-IDF scores are incorporated with Named Entity Recognition method to identify the major keywords of the original texts. To enforce the appearance of those keywords in the generated titles, the specific Teacher Forcing mechanism combined with the language model technique are employed. We have tested our approaches with real datasets and obtained promising initial results, on both metrics of machine and human perspectives.

Keywords: *Sequence to sequence, Attention Mechanism, Named Entity Recognition, TF-IDF, Language Model, Teacher Forcing, Pointer Generator Network.*

ENHANCING SECURITY AND ROBUSTNESS FOR SDN-ENABLED CLOUD NETWORKS

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ABSTRACT

Software-Defined Networking is an emerging network architecture which promises to solve the limitations associated with current cloud computing systems based on traditional network. The main idea behind SDN is to separate control plane from networking devices, thereby providing a centralized control layer integrable to cloud-based infrastructure. The integration of SDN and Cloud Computing brings immense benefits to network deployment and management, however, this model still faces many critical challenges with regards to availability, scalability and security. In this study, we present a security and robustness SDN-Enabled Cloud model using OpenStack and OpenDaylight. In particular, we design and implement a security clustering-based SDN Controller for monitoring and managing cloud networking, and a hardware platform to accelerate packet processing in virtual switches. We evaluate our proposed model on a practical cloud testbed consisting of several physical and virtual nodes. The experiment results show that the SDN controller cluster significantly improve robustness for the network even in case of being attacked by abnormal network traffic; while the hardware-accelerated switches can be operated in high-performance and well-adapted to the cloud environment.

Keywords: *Cloud Computing, SDN, OpenStack, OpenDaylight, Network Security.*

UNBIASED PAIRWISE APPROACH TOWARD LEARNING-TO-RANK: AN EMPIRICAL STUDY

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ABSTRACT

With the bloom of information technology in recent decades, people are constantly being exposed to a huge amount of information. Learning-to-rank comes out as one of the solutions to ease out the mentioned obstacle by trying to rearrange objects according to their degrees of importance or relevance. This solution usually applies machine learning techniques to construct ranking models in information retrieval systems. The aim of this study is to explore and experiment the existing learning-to-rank approaches with real-life logs data. The study also includes estimating and minimizing the bias noise found in the click-through data of the recorded logs. Evaluation results have presented the advantage and disadvantage of the experimented approaches in realistic settings.

Keywords: *Unbiased Pairwise, Learning-to-Rank, Machine Learning, Click Logs.*

REAL-TIME FACE DETECTION AND HUMAN TRACKING SYSTEM ON FPGA CYCLONE-V

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ABSTRACT

Face detection in image sequence (real-time video stream) has been an active research area in the computer vision field in recent years due to its potential applications such as surveillance cameras, human computer interfaces, smart rooms, intelligent robots and biomedical image analysis. Face detection is a process that determines whether an image has a face or not. In this paper, an embedded system for detecting and tracking human faces in real-time video stream implemented on FPGA DE10-NANO is proposed. The system can be divided into two parts: data streaming, data processing. Experimental results show that the system is capable of accurately detecting faces of up to 5 different people at a distance of up to 1.5 meters from the camera, coexisting in the same frame in resolution of 320x240 pixels with a detection speed of only several hundred milliseconds prove the feasibility of the system. A comparison with similar existing projects will be discussed for evaluation and conclusion as well.

Keywords: *Embedded system, human tracking system, face detection system, FPGA.*

TWO-PHASE DEFECT DETECTION USING CLUSTERING AND CLASSIFICATION METHODS

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ABSTRACT

Autonomous fault management of network and distributed systems is a challenging research problem and attracts many research activities. Solving this problem heavily depends on expertise knowledge and supporting tools for monitoring and detecting defects automatically. Recent research activities have focused on machine learning techniques that scrutinize system output data for mining abnormal events and detecting defects. This paper proposes a two-phase defect detection for network and distributed systems using log messages clustering and classification. The approach takes advantage of K-means clustering method to obtain abnormal messages and random forest method to detect the relationship of the abnormal messages and the existing defects. Several experiments have evaluated the performance of this approach using the log message data of Hadoop Distributed File System (HDFS) and the bug report data of Bug Tracking System (BTS). Evaluation results have disclosed some remarks with lessons learned.

Keywords: *Defect Detection, Clustering, Classification, HDFS Logs, BTS Bugs, Network Fault Management.*



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